Final Assessment Test (FAT) - JUNE/JULY 2023

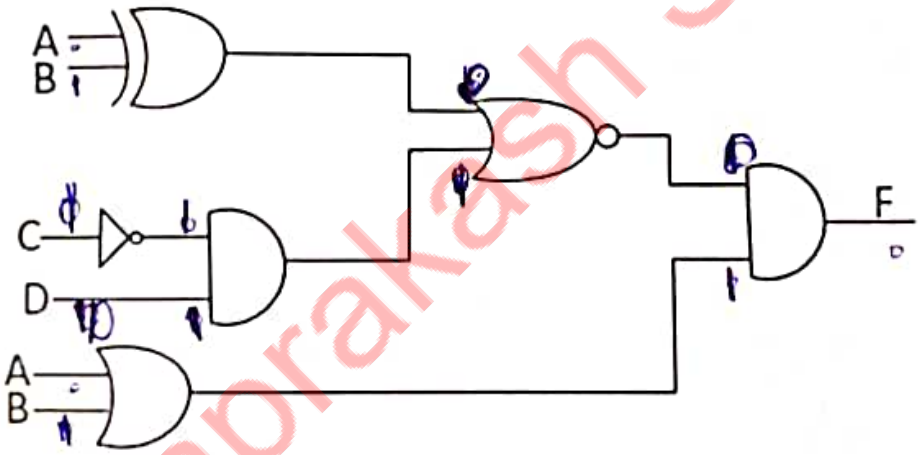
Programme	B.Tech.	Semester	Winter Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. ASHOK	Slot	B1+TB1
		Class Nbr	CH2022232300193
Time	3 Hours	Max. Marks	100

Section A (10 X 10 Marks)
Answer All questions

01. Design a full-adder circuit and implement the same using (a) suitable decoder (b) NAND gates only. [10]

02. (a) Simplify the given Boolean function, F (A, B, C, D) = Σ (1,4,6,12,14) in SOP form using K-Map. [10]

(b) Consider the combinational circuit shown in Figure. Determine the truth table for the output, F as a function of the four inputs.



03. Design a logic circuit with 4 inputs A, B, C, D that will produce the output '1', only when two adjacent input variables are 1. Variables A and D are also treated as adjacent. Implement the circuit using universal logic gates for both the cases (SOP and POS). [10]

04. Implement the given Boolean function using an 8:1multiplexer considering D as input and A, B, C as the selection lines. [10]

$$F(A,B,C,D) = A\bar{B} + BD + \bar{B}C\bar{D}$$

05. Design a 3 x 2 and 3 x 3 binary multiplier circuit using adders. [10]

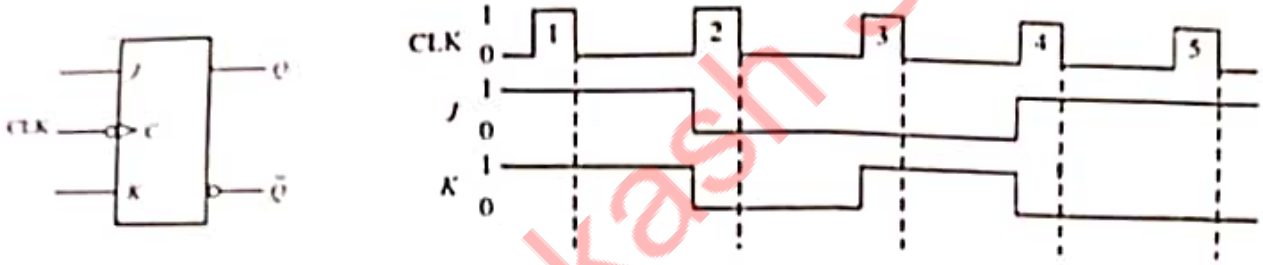
06. Obtain the truth table for a 3-bit magnitude comparator and draw the logical diagram for the same. [10]

07. Design a synchronous counter for the sequence : 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip flops [10]

08. The waveforms in Figure are applied to the J, K, and clock inputs of a J-K flip flop. [10]

(a) Determine the Q output, assuming that the flip-flop is initially RESET.

(b) Determine the Q output of the J-K flip-flop if the J and K inputs in Figure are inverted.



09. Design a Moore state machine based overlapping sequence detector to detect the sequence '111'. Implement the sequence detector using one J-K flip flop and one D flip flop. **[10]**

10. Compare PLA and PAL. Implement the following two functions using PLA. **[10]**

F1 = A B' + A C + A' B C'

F2 = (A C + B C)'

VIT

Reg. No. : 22BCE1359

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	B.Tech.	Semester	Winter Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Mohamed Imran A	Slot	B1+TB1
		Class Nbr	CH2022232300550
Time	3 Hours	Max. Marks	100

Section I (7 X 10 Marks)
Answer All questions

01. For the given Boolean function, [10]

$F(W, X, Y, Z) = X\bar{Y}Z + \bar{X}\bar{Y}Z + \bar{W}XY + W\bar{X}Y + WXY$

(a) Obtain the truth table of F and represent the function with minterms.

(b) Use Boolean algebra to simplify the function and realize the circuit using NAND gates

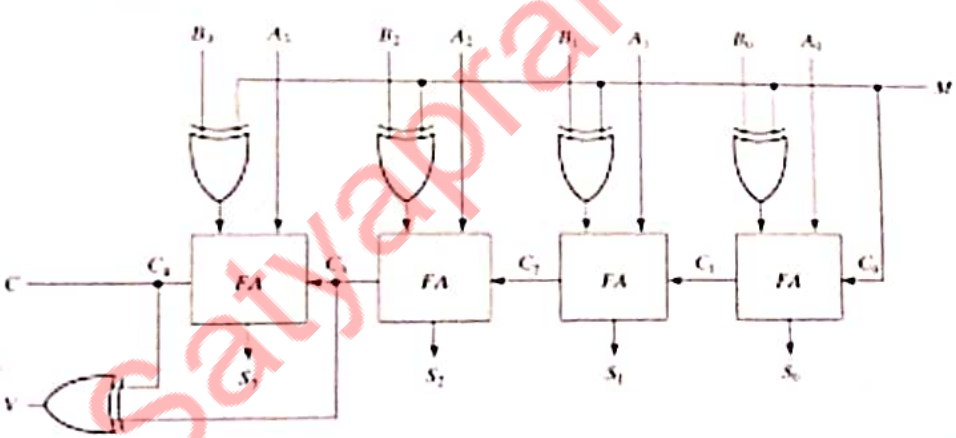
(c) Write a Verilog code to implement the function using structural modelling.

02. Design a combinational circuit to generate EVEN parity and ODD parity. Write the truth table with $(ABCD)$ as inputs and X(Even) , Y (Odd) as outputs. [10]

(a) Implement the output X using 4×1 multiplexer.

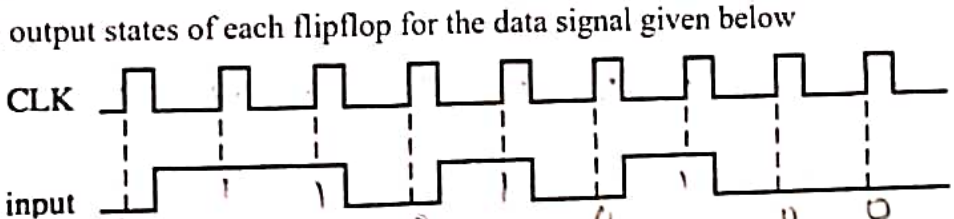
(b) Implement the output Y using 3×8 decoder.

03. Comprehend the circuit shown below and find the outputs $(S_3S_2S_1S_0)$, C and V for $M = 0$ and $M = 1$. Assume $A = +6$ and $B = +4$. What does V indicate? Validate your answer with the calculations. [10]



04. (a) The sequence 1011 is applied to the input of a 4-bit shift register(SISO) that is initially cleared. What is the state of the shift register after three clock pulses?Explain with timing diagram/table. [10]

(b) Draw the output states of each flipflop for the data signal given below



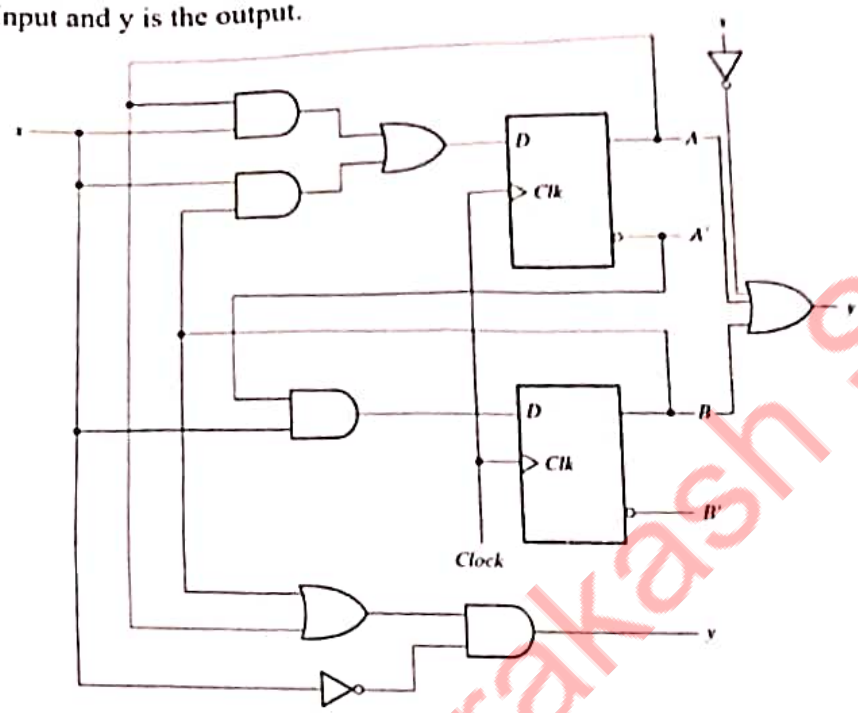
05. Design and draw the state diagram of a FSM to detect two sequences 1010 and 110 for the following cases: [10]

(a) Mealy model with overlapping states

(b) Moore model with non overlapping states.

06. Design an modulo 8 asynchronous counter using negative edge triggered JK Flip Flop [10]
(a) the counter should count with a truncated sequence 2,3,4,5,6.
(b) draw the timing diagram and verify the output.

07. Derive the state table and the state diagram of the sequential circuit shown below, where x is the input and y is the output. [10]



Section II (2 X 15 Marks)
Answer All questions

08. The arithmetic operation $C = A * B$ is performed on a digital system. [15]
(a) Tabulate the calculation steps using Booth Algorithm, if $A = +5$ and $B = -4$
(b) Write the Verilog code for implementing the same operation with Array Multiplier using dataflow modelling.

09. Implement the combinational circuit [15]
$F1(W, X, Y, Z) = \sum(2, 12, 13)$,
$F2(W, X, Y, Z) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$,
$F3(W, X, Y, Z) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$,
$F4(W, X, Y, Z) = \sum(1, 2, 8, 12, 13)$
(a) using Programmable Logic Array (PLA).
(b) using Programmable Array Logic (PAL).

VIT

Reg. No. : 22BPS1013

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	B.Tech.	Semester	Winter Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Angeline Ezhilarasi G	Slot	B2+TB2
		Class Nbr	CH2022232300528
Time	3 Hours	Max. Marks	100

Section I (4 X 10 Marks)
Answer All questions

01. For the given Boolean function, [10]

$F(X,Y,Z) = X\bar{Y}Z + \bar{X}Y\bar{Z} + XY + \bar{X}\bar{Y}$

(a) Obtain the truth table of F and represent the function with minterms and maxterms

(b) Use Boolean algebra to simplify the function and write a Verilog code to implement the function using structural modelling.

02. Design a 3-bit code converter to convert binary digits to gray code. Draw the truth table with inputs as ABC and the outputs as XYZ. [10]

(a) Implement the output X using 4×1 multiplexer and Y using 2×4 decoder.

(b) Implement the output Z using NAND gates.

03. A system takes two inputs $A = A_1A_0$ and $B = B_1B_0$. [10]

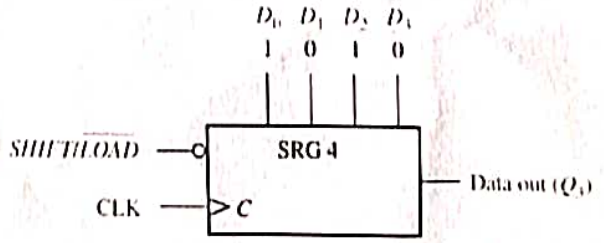
(a) Design a logic circuit to check if the two inputs are equal.

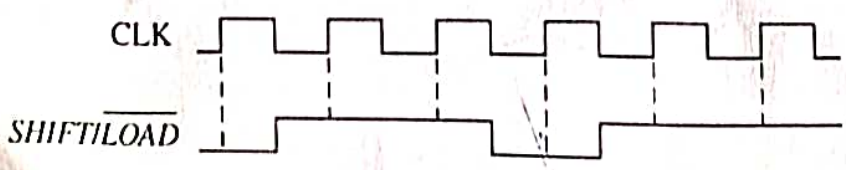
(b) Design and write the Verilog code to perform the arithmetic operation $A \times B$ using dataflow modelling.

04. Identify the sequential circuit represented by the symbol shown below. What does $SHIFT/\overline{LOAD}$ indicate? [10]

(a) Tabulate the outputs for 6 clock cycles for the inputs $D_0 = 1, D_1 = 0, D_2 = 1, D_3 = 0$

(b) Develop the output waveform Q_3





Section II (4 X 15 Marks)

Answer All questions

05. A control logic is developed for a traffic signal at the intersection of a busy main road and lightly used crossroad. There is a sensor to detect vehicles waiting on the crossroad. The sensor sends a signal X as input to the controller. $X = 1$ if there are vehicles on the crossroad; otherwise, $X = 0$. Assume initially that the main road green light is ON and the crossroad red light is OFF and there is a constant delay between change over from Yellow to Green/Red. [15]

(a) Identify and name four unique states to design the controller and draw the state diagram with an efficient state assignment.

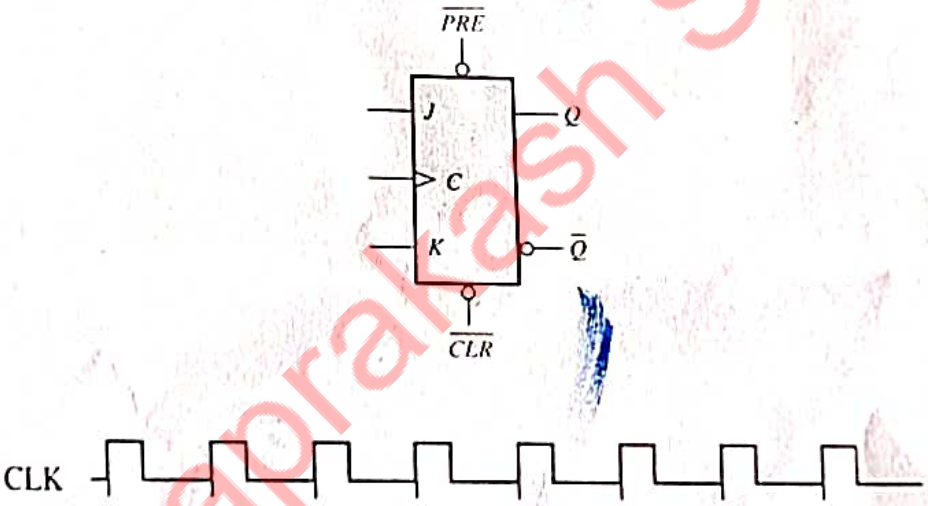
(b) Design a synchronous delay circuit to count down from 5 to 0 using D Flip Flops.

06. How many flip-flops are required to design a modulo-10 counter? Using the flip-flop shown below. [15]

(a) design a modulo-8 ripple down counter. Validate the output by timing diagram.

(b) modify the circuit to start the counter at 6 and end at 3.

(c) If the input clock is 64 kHz, what will be clock frequency of the last flip flop in the design.



07. Design and draw the state diagram of a FSM to detect two sequences 1010 and 110 for the following cases: [15]

(a) Mealy model with overlapping states. If state reduction is possible, draw the reduced state diagram.

(b) Moore model with non-overlapping states.

08. A combinational logic circuit has the following outputs. [15]

$F_1 = \sum(0, 2, 3, 4)$ and $F_2 = \sum(1, 2, 3, 6)$

(a) Implement the circuit using a suitable Programmable Logic Array (PLA). Specify the size of the PLA used.

(b) How will you implement the same circuit in a Programmable Array Logic (PAL) which has 3 inputs. 2 outputs and 2 divisions of 2 wide AND array.

VIT

Reg. No. : 22BRS1135

Programme	B.Tech.		
Course Title	DIGITAL SYSTEMS DESIGN	Semester	Winter Semester 2022-23
Faculty Name	Prof. Nithya Venkatesan	Course Code	BECE102L
Time	3 Hours	Slot	B2+TB2
		Class Nbr	CH2022232300522
		Max. Marks	100

Final Assessment Test (FAT) - JUNE/JULY 2023

Section 1 (10 X 10 Marks)
Answer All questions

01. A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations. [10]
    (i) A is True , B is False
    (ii) A is False, C is True
    (iii) A, B, C are False
    (iv) A, B, C are True
    (a) Write the Truth table for F. Use the convention True=1 and False = 0.
    (b) Write the simplified expression for F in SOP form.
    (c) Write the simplified expression for F in POS form.
    (d) Draw logic circuit using minimum number of 2-input NAND gates.
02. Determine a minimal SOP and POS expression for the following Boolean functions together with the don't care conditions d using four variable k map. Note that the don't care conditions have to be set to one value for the SOP solution and the other for the POS expression. [10]
    $F(w,x,y,z) = \Sigma(1,9,10,11,12,13,14,15)$
    $d(w,x,y,z) = \Sigma(3,5,8)$
03. Write the Verilog code for a parity generator circuit and draw its logic diagram. [10]
04. You wish to detect only the presence of the codes 1010,1100,0001 and 1011. An active HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be low. [10]
05. Discuss the concept of an adder whose carry propagation delays are eliminated. Draw its block diagram. [10]
06. Design a non- sequential synchronous counter using D Flip- Flops to count the sequence 6, 0, 7,1,3,6,0,7,1,3, -- so on. The loop for the undesired states must also be designed. [10]
07. (i) The initial contents of the 4-bit serial-in-parallel out, right-shift, Shift Register shown in the given Figure 1 is 0110. After six clock pulses are applied, contents of the Shift Register will be [10]

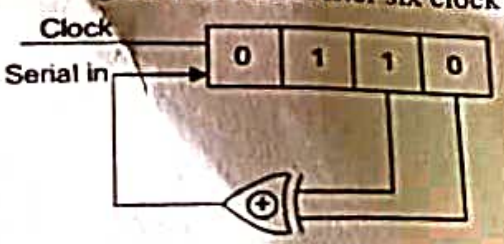


Figure 1

Explain and draw the necessary register diagram for every clock pulse. (5 marks)

(ii) Explain the working of a 3 bit Asynchronous up-counter. Write a Verilog HDL code for the same. (5 marks)

08. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. Design a serial sequence detector which allows "overlapping" and detects the pattern "0101". Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using JK flip flop. [10]

09. Construct a Moore machine that prints 'a' whenever the sequence "1001" is encountered in any input binary string. Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using D flip flop. [10]

10. Implement the following boolean expression using Programmable Logic Array (PLA) [10]

$$F_1(x,y,z) = \sum_m (1,3,4,5,7)$$

$$F_2(x,y,z) = \sum_m (1,4,5,6)$$

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	**B.Tech.**	Semester	**Winter Semester 2022-23**
Course Title	**DIGITAL SYSTEMS DESIGN**	Course Code	**BECE102L**
Faculty Name	**Prof. Prathiba A**	Slot	**D1+TD1**
		Class Nbr	**CH2022232300124**
Time	**3 Hours**	Max. Marks	**100**

SECTION 1 (4 X 5 Marks)
Answer All questions

01. Identify the functionality of the following circuit shown in Fig.1. and depict the output sequence obtained for the first eight clock cycles, assume the 'initial states as 0000'. [5]

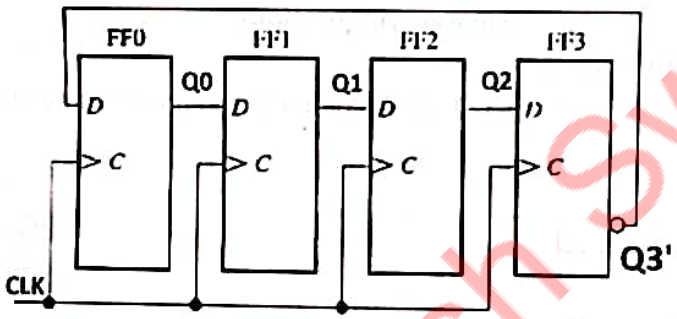


Fig.1

02. Simplify the expression to minimum number of literals using Boolean laws [5]

$$f = ABCD + \bar{A}BCD + \overline{BC}$$

03. Implement the following Boolean function with PLA logic [5]

$$F(A, B, C, D) = \Sigma(0, 4, 8, 9, 10, 11, 12, 14)$$

04. Differentiate = Vs <= assignment statement with suitable examples [5]

SECTION 2 (5 X 10 Marks)
Answer All questions

05. Determine the minimum-cost SOP and POS expressions for the function; also draw the diagrams using only NOR for POS simplified expression. [10]

$$f(x_1, x_2, x_3, x_4) = \sum m(4,6,8,10,11,12,15) + D(3,5,7,9)$$

06. Design a combinational circuit which has three inputs A,B,C and two outputs Z1, Z2 with the following specifications [10]

- If C = 0, Z1 follows B and Z2= A OR B.
- If C= 1, Z1 = A XOR B and Z2 = A AND B.

a) Use a decoder and OR gates to implement the function.

b) Use a 8:1 multiplexer to implement the function.

07. Suggest an adder which has less latency in comparison against the ripple carry adder and explain the same in detail with circuit diagram. [10]

08. Write the Verilog HDL code for the circuit shown in Fig. 2. [10]

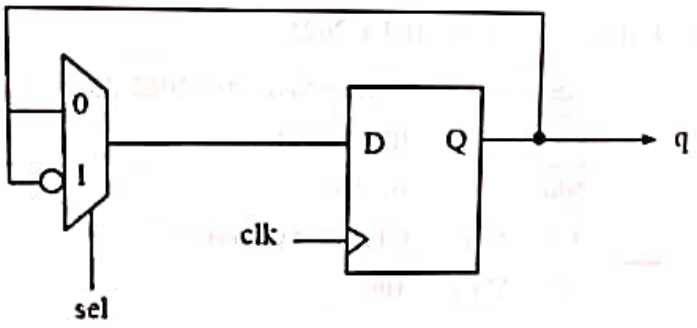


Fig. 2

09. Write the Verilog code for a "101" non-overlapping sequence detector's state diagram using Mealy model. [10]

SECTION 3 (2 X 15 Marks)
Answer All questions

10. (i) Design a 2-bit comparator using gates [15]
(ii) For the given input waveform in Fig.3, draw the output for D positive edge triggered flip flop

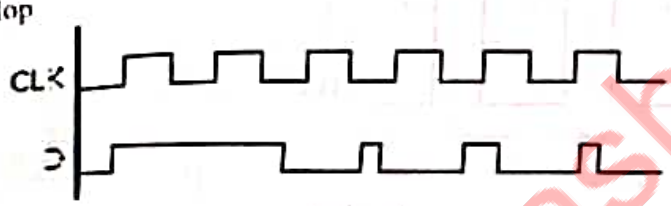


Fig.3

11. Design a synchronous counter using JK flip flop that counts the sequence 2, 3, 5, 2, 3, 5,..... [15]

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Reg. No. : Aryan. 22BRS1143

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	**B.Tech.**	Semester	**Winter Semester 2022-23**
Course Title	**DIGITAL SYSTEMS DESIGN**	Course Code	**BECE102L**
Faculty Name	**Prof. Ravi Tiwari**	Slot	**B2+TB2**
		Class Nbr	**CH2022232300195**
Time	**3 Hours**	Max. Marks	**100**

Section 1 (10 X 10 Marks)
Answer All questions

01. A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations. [10]

(i) A is True , B is False 1 0

(ii) A is False, C is True 0 0 1

(iii) A, B, C are False

(iv) A, B, C are True

(a) Write the Truth table for F. Use the convention True=1 and False = 0.

(b) Write the simplified expression for F in SOP form.

(c) Write the simplified expression for F in POS form.

(d) Draw logic circuit using minimum number of 2-input NAND gates.

02. Determine a minimal SOP and POS expression for the following Boolean functions together with the don't care conditions d using four variable k map. Note that the don't care conditions have to be set to one value for the SOP solution and the other for the POS expression. [10]

F(w,x,y,z) = Σ(1,9,10,11,12,13,14,15)

d(w,x,y,z) = Σ(3,5,8)

03. Write the Verilog code for a parity generator circuit and draw its logic diagram. [10]

04. You wish to detect only the presence of the codes 1010,1100,0001 and 1011. An active HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be low. [10]

05. Discuss the concept of an adder whose carry propagation delays are eliminated. Draw its block diagram. [10]

06. Design a non- sequential synchronous counter using D Flip- Flops to count the sequence 6, 0, 7,1,3,6,0,7,1,3, -- so on. The loop for the undesired states must also be designed. [10]

07. (a) The initial contents of the 4-bit serial-in-parallel out, right-shift, Shift Register shown in the given Figure 1 is 0110. After six clock pulses are applied, contents of the Shift Register will be [10]

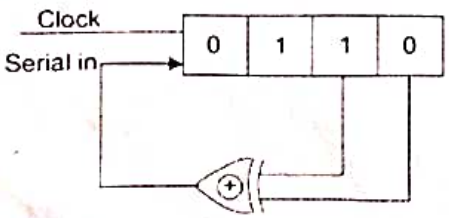


Figure 1

Explain and draw the necessary register diagram for every clock pulse. (5 marks)

(ii) Explain the working of a 3 bit Asynchronous up-counter. Write a Verilog HDL code for the same. (5 marks)

08. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. Design a serial sequence detector which allows "overlapping" and detects the pattern "0101". Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using JK flip flop. [10]

09. Construct a Moore machine that prints 'a' whenever the sequence "1001" is encountered in any input binary string. Draw the respective state diagram, state table, transition table, derive the characteristic equations and implement the FSM using D flip flop. [10]

10. Implement the following boolean expression using Programmable Logic Array (PLA) [10]

$$F_1(x, y, z) = \sum_m (1,3,4,5,7)$$

$$F_2(x, y, z) = \sum_m (1,4,5,6)$$

VIT Vellore Institute of Technology

Reg. No. : 22BEC1074

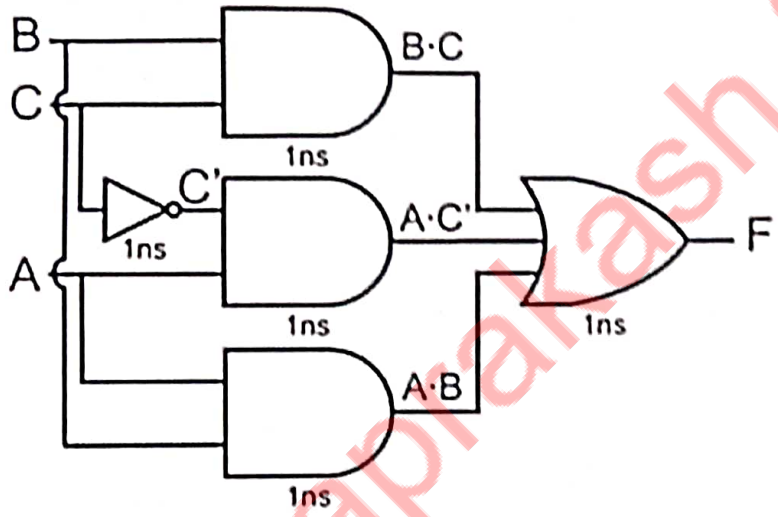
Final Assessment Test (FAT) - November/December 2023

Programme	B.Tech.	Semester	FALL SEMESTER 2023 - 24
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Prathiba A	Slot	B1+TB1
		Class Nbr	CH2023240100535
Time	3 Hours	Max. Marks	100

Part-A (5 X 5 Marks)
Answer all questions

01. Draw the CMOS logic circuit for the given expression [5]
F= (A (B C + D))'

02. Write the gate level Verilog model for the following circuit. Also write the test bench for your design [5]



03. Write a structural modelling Verilog code to add two 4-bit numbers using appropriate adders [5]

04. Design a parity checker circuit for 4-bit data which is to be transmitted by computer X along with an even parity bit (total 5 bits). The receiving computer Y will generate an error bit, E = 1 if the 5 bit data received has an odd parity; otherwise, E = 0. Draw the logic diagram for parity checking using XOR gates [5]

05. Implement a 16:1 MUX logic by using combination of 4:1 only MUX. Identify the selection pattern "$S_0S_1S_2S_3$" to select the 13th data input at the output [5]

Part-B (6 X 10 Marks)
Answer all questions

06. (a) Simplify the given Boolean function along with don't care condition 'd' using K-map and express in SOP and POS forms. [10]
$F(A, B, C, D) = \Sigma_m (1, 3, 7, 11, 15) + \Sigma_d (0, 2, 5)$
(b) Draw the logic circuit diagram using only NOR gates for the above simplified Boolean expression.

07. Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable high for an addressable LED display. Write the Verilog code for the same using gate level modelling [10]

08. Suggest a way to reduce the carry propagation delay in a 4-bit parallel adder by using suitable logic. Assume two 4-bit inputs A and B. Justify your answer using design equations and logic diagram. [10]

09. Design a BCD counter using JK flip flops [10]

10. A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations [10]

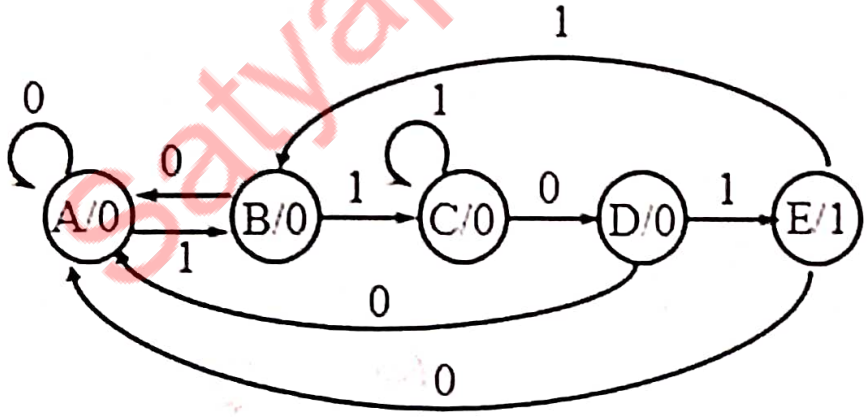
$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

i) List the state table for the sequential circuit
ii) Draw the state diagram
iii) Draw the logic diagram of the circuit

11. Draw the PAL and PLA circuit for the simplified four Boolean functions as listed below. [10]
F1(x, y, z) = Σ(0, 1, 5, 7)
F2(x, y, z) = Σ(2, 4, 5, 6)
F3(x, y, z) = Σ(0, 1, 2, 3, 4)
F4(x, y, z) = Σ(3, 6, 7)

Part-C (1 X 15 Marks)
Answer all questions

12. Determine the state table and excitation table for a non-overlapping Moore Sequence Detector for the sequence "1101" as given in the below figure and write the Verilog code for this sequence detector. Use D flip flop for your design [15]



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