Reg. No.:

Name :

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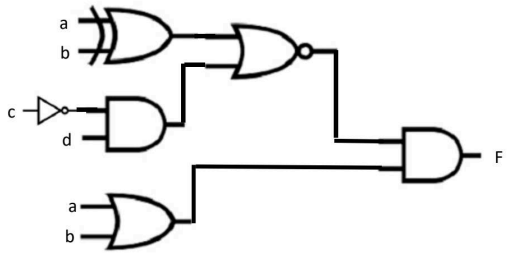
Continuous Assessment Test I – September 2022

Programme	:	**BAI/BCE/BPS/BRS**	Semester	:	**FS 2022-23**
Course	:	**Digital System Design**	Code	:	**BECE102L**
			Class Nbr	:	
Faculty	:		Slot	:	**E1+TE1**
Time	:	**90 Minutes**	Max. Marks	:	**50**

Answer ALL the questions

Q.No.	Sub-division	Question Text	Marks
1.		a) Reduce the following Boolean expressions WXY'Z+W'XZ+WXYZ b) Express the given function as in a) in POS form	**[2]** + **[3]**
2.		F(A, B,C,D)= π(1,4,6,12,14) i) Simplify the given Boolean function in SOP form using K-Map. ii) Draw a CMOS logic circuit for this simplified expression. (Assume both true and complementary inputs are available)	**[5]** + **[5]**
3.		Consider the combinational circuit shown  Determine the truth table for the output F as a function of the four inputs.	**[5]**
4.		For the functionality defined by the minterms $F1 = \sum (1,2,3,6,8,9,10,12,13,14)$, write the Verilog program using (a)Behavioral and (b) dataflow modelling	**[10]**
5.		Identify the errors in the Verilog program given below for the Boolean expression $F = (A + \overline{CD})(\bar{A} + B)$. *Module test (a, b, c, d, F)* *input a,b,c,d;* *output F;* *reg f1,f2,f3,f4;* *not g1(f1,a);*	**[10]**

		nand g2(f2,c,d); *or g3(f1,f3,b);* *or g3(f4,a,f2);* *nand (F, f3,f4)* *end module* Check for both syntactic and logical errors, Correct it.	
6.		Design a full-subtractor circuit and implement the same a) Using suitable decoder. b) Using NAND only	**[10]**
		Total Marks	**[50]**

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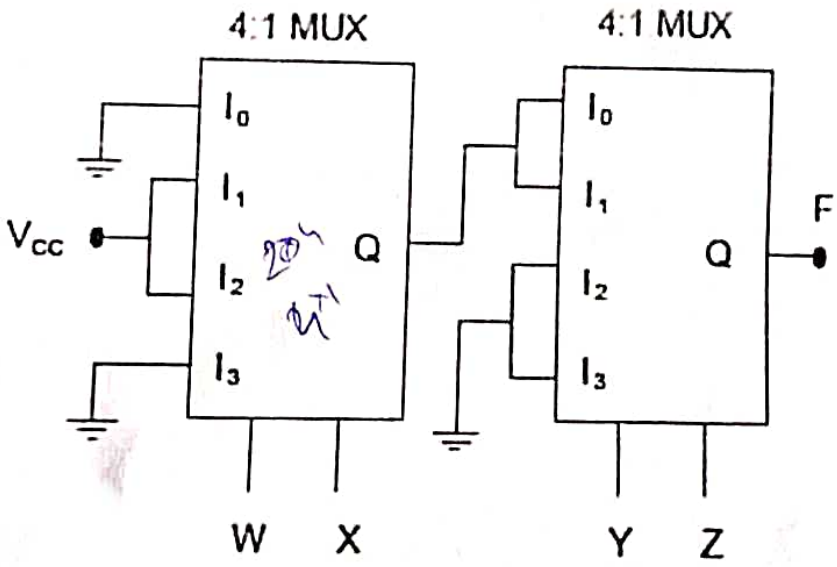
Continuous Assessment Test - 1 (CAT 1) – March 2023

ne	: B. Tech CSE & Splns	Semester	:	Winter 22-23
	: Digital Systems Design	Code	:	BECE102L
		Slot	:	B1+TB1
	: Dr. Ashok Mondal Dr. Deepa T Prof. Deepa M Dr. Meera P S Dr. Sriramalakshmi P Dr. Subbulekshmi D	Class Nbr	:	CH2022232300193 CH2022232300530 CH2022232300191 CH2022232300559 CH2022232300535 CH2022232300526
	: 1.5 hours	Max. Marks	:	50

Answer ALL Questions

Sub. Sec.	Question Description	Marks
	Simplify the following expressions using Boolean algebra. a) $Y = (M + N)(\bar{M} + P)(\bar{N} + P)$ b) $\overline{\overline{AB}(CD + \bar{E}F)(\overline{AB} + \overline{CD})}$ c) $(B + BC)(B + \bar{B}C)(B + D)$ d) $Y = A\bar{B}C + (\bar{B} + \bar{C})(\bar{B} + \bar{D}) + \overline{A + C + D}$	10
	Reduce the logic function F(A,B,C,D) = ∑m (1,2,3,4,7,11,13) + d (9,15) using K- map in SOP form. Implement the minimized expression using only NAND gates.	10
	Design a digital system whose output is defined as logically low if the 4 bit input binary number is a multiple of 3; otherwise, the output will be logically high. The output is defined if and only if the input binary number is greater than 2. Draw the logical diagram for the simplified expression for the above system.	10
	For the Boolean expression, F(A,B,C,D) = (A+B'+D) (A'+B+C') (B+C+D'), a) draw the truth table and mark the outputs correctly. Realize the expression using b) 3:8 decoders with active high enable. c) 8:1 multiplexer and external gates (Select lines: A, B, C). d) 4: 1 multiplexer and external gates (Select lines: A, B).	15

5 For the circuit given below, find the expression for F.



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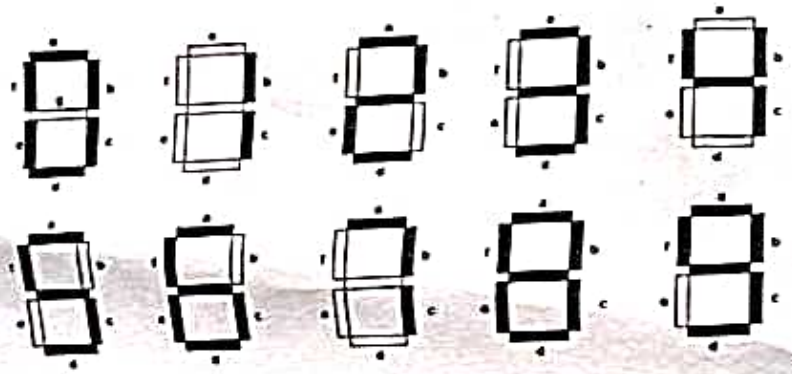
Continuous Assessment Test I- March 2023

Programme	:	B.Tech CSE	Semester	:	Winter 2022-23
Course	:	Digital System Design	Code	:	BECE102L
Faculty	:	A. Mohamed Imran	Slot	:	B1+TB1
			Class Number	:	CH2022232300550
Time	:	$1\frac{1}{2}$ Hours	Max. Marks	:	50

Answer ALL Questions

1. In a seven segment display as shown below, each of the seven segments are activated for various digits. The input is given in Binary Coded Decimal format.
   (a) Design a combinational circuit to activate the segment a. Find the boolean function in SOP form and implement the circuit using a 3 to 8 line decoder. (8)
   (b) Obtain the minimal POS expression for segment e. Realize the circuit using NOR gate. (8)



2. Design a combinational circuit to compare any two 3-bit numbers and specify if $(A = B)$ or $(A < B)$ or $(A > B)$. (8)

3. Design a logical circuit that generates the 2's complement of a given 3 bit binary number. Let A, B, C be the inputs and X, Y, Z be the outputs. (8)
   (a) Simlify the boolean fuention X using boolean algebra
   (b) Implement the function Z using 4 × 1 multiplexer. Use A, B as selection lines.

4. The 8 × 1 multiplexer has inputs A, B and C connected to the selection inputs S2, S1 and S0 respectively. The data inputs I0 through I7 are as follows: (8)

$$I2 = 0; I0 = I1 = I3 = 1; I4 = I6 = I7 = D; I5 = \bar{D}$$

Form the truth table and identify the boolean function that the multiplexer implements.

5. Compute the output of a 4-bit Booth multiplier taking $A = 6$ as the multiplicand and $B = -6$ as the multiplier. (10)

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Continuous Assessment Test I - March 2023

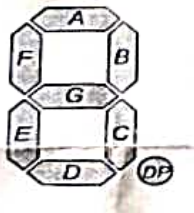
Programme	:	B.Tech CSE	Semester	:	Winter 2022-23
Course	:	Digital System Design	Code	:	BECE102L
Faculty	:	G. Angeline Ezhilarasi	Slot	:	B2+TB2
			Class Number	:	CH20222323300528
Time	:	$1\frac{1}{2}$ Hours	Max. Marks	:	50

Answer ALL Questions

1. In a seven segment display as shown below, each of the seven segments are activated for various digits. The input is given in Binary Coded Decimal format.

   (a) Design a combinational circuit to activate the **segment B** such that the circuit can be realized with NOT-AND-OR as gate levels . Find the boolean function and implement the circuit using a 3 to 8 line decoder. (8)

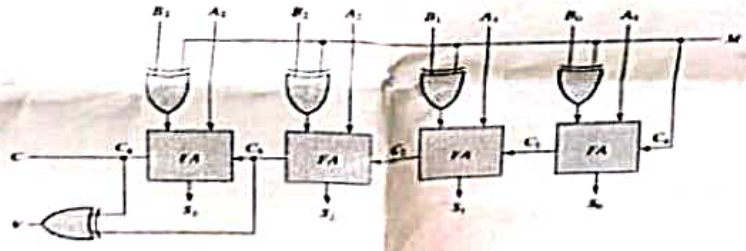
   (b) Obtain the minimal POS expression for **segment C**. Realize the circuit using a suitable multiplexer. (8)



2. In a data transmission system, a 2 bit data is transmitted with an odd parity using a parity generator. At the receiving end it is checked for error using a parity checker. Design the parity generator and checker. Simplify the functions using boolean algebra. (8)

3. Design a two bit priority encoder with high priority given to LSB using combinational circuits. $(MSB - D_1, LSB - D_0)$ (8)

4. Comprehend the circuit shown below and find the outputs $(S_3S_2S_1S_0)$, C and V for $M = 0$ and $M = 1$. Assume $A = +6$ and $B = +4$. What does V indicate? Validate your answer with the calculations. (8)



5. Compute the output of a 3-bit Booth multiplier taking $A = 2$ as the multiplicand and $B = -3$ as the multiplier. (10)

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Continuous Assessment Test (CAT-1) – March 2023

Programme	:	B.Tech (CSE)	Semester	:	Winter 2022-2023
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2022232300522 CH2022232300543 CH2022232300532, CH2022232300556, CH2022232300195, CH2022232300524
Faculty	:	Dr.Nithya Venkatesan, Dr.B.Sri Revathi, Dr.G.Kanimozhi, Dr.S.Angalaeswari, Dr.Ravi Tiwari, Prof. Mohammed Aneesh	Slot	:	B2+TB2
Time	:	90 minutes	Max. Marks	:	50

Answer **Any 5** of the following Questions

S.No.	Question Description	Marks
1.	An assembly line has 3 fail safe sensors and one emergency shutdown switch. The line should keep moving unless any of the following conditions arise: (i) If the emergency switch is pressed (ii) If the sensor1 and sensor2 are activated at the same time. (iii) If sensor 2 and sensor3 are activated at the same time. (iv) If all the sensors are activated at the same time. Draw the truth table and implement a combinational circuit for the above case using only NAND gates. How many minimum number of 2 input NAND gates are required?	[10]
2.	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations : A is False, B is True A is False, C is True A, B, C are False A, B, C are True (i) Write the Truth table for F. Use the convention, True=1 and False = 0. (ii) Write the simplified expression for F in SOP form.	[10]

(iii) Write the simplified expression for F in POS form.

(iv) Draw logic circuit using minimum number of 2-input NOR gates.

3. Design and implement a full subtractor in Verilog using gate level modeling. Draw necessary truth table and logic diagrams. [10]

4. Implement the function F (A,B,C,D) = Σm(2,3,4,5,6,7) using a decoder without using OR gates. [10]

5. Implement a full adder using two 4×1 multiplexers. Draw the truth table and necessary k-maps. [10]

6. Reduce the following expression using K map both in SOP and POS and implement them using basic gates. Comment which simplification uses the minimum number of gates. [10]

F = Σm(0,1,2,8,9,10,11,13,14,15).

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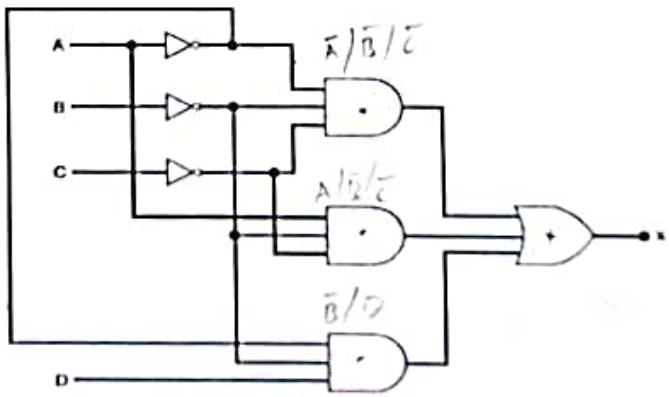
Continuous Assessment Test I – March 2023

Programme	:	B.Tech	Semester	:		WS 2022-23
Course	:	Digital System Design	Code	:		BECE102L
			Class Nbr	:		CH2022232300125
Faculty	:	Dr.K.Srivatsan	Slot	:		D1
Time	:	90 Minutes	Max. Marks	:		50

Answer ALL the questions

Q No	Sub-division	Question Text	Marks
1.		A logic 'voter' circuit has 4 inputs ***a***, ***b***, ***c***, ***d*** and one output ***v***. The output is to be logic 1 if any 3 or all 4 inputs are at logic 1. Draw a truth table map for each input and hence write down the simplified Boolean equations using K-Map method of reduction. Design a circuit using NOR gates to satisfy this requirement.	[10]
2.		Draw a CMOS logic circuit for the given expression. (Assume both true and complementary inputs are available) $F = (A + \overline{CD})(\bar{A} + B)$.	[5]
3.		Write the Boolean expression for output x in Figure 1. Determine the value of x for all possible input conditions in a truth table.  Figure 1	[5]
4.	i.	Simplify the given function F1=∑ (1, 5, 6, 7, 11, 12, 13, 15)	
	ii.	For the original and the simplified expression, write the Verilog HDL code using dataflow modelling.	[5] + [5]
5.		Write a gate level Verilog code for the schematic shown in Figure 2 and write a test bench for the same.	[10]

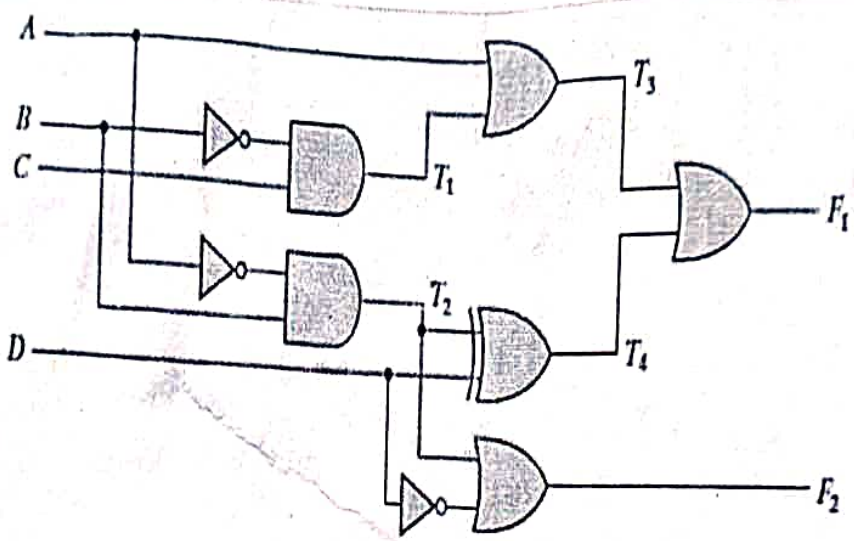


Figure 2

6. Design a 4:2 priority encoder. Also discuss the differences between encoder and priority encoder? [10]

Total Marks [50]

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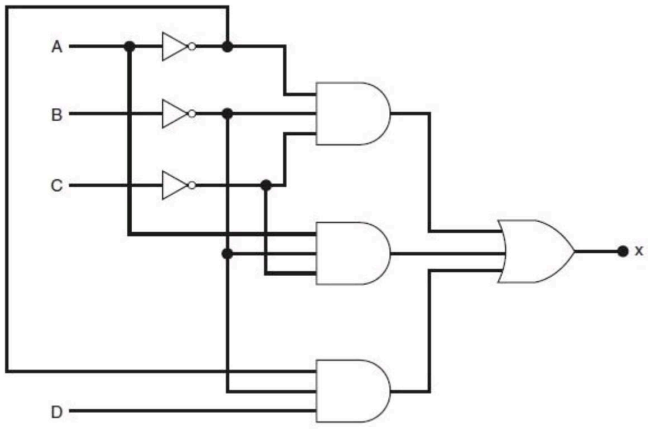
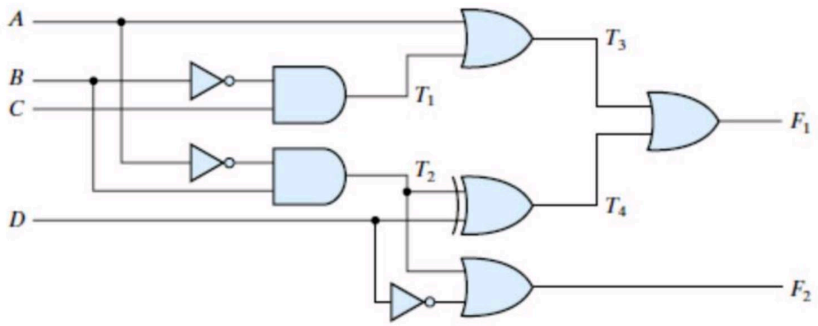
Continuous Assessment Test I – March 2023

Programme	:	**B.Tech**	Semester	:		**WS 2022-23**
Course	:	**Digital System Design**	Code	:		**BECE102L**
			Class Nbr	:		CH2022232300125
Faculty	:	**Dr.K.Srivatsan**	Slot	:		**D1**
Time	:	**90 Minutes**	Max. Marks	:		**50**

Answer ALL the questions

Q.No.	Sub-division	Question Text	Marks
1.		A logic 'voter' circuit has 4 inputs ***a, b, c, d*** and one output ***v.*** The output is to be logic 1 if any 3 or all 4 inputs are at logic 1. Draw a truth table map for each input and hence write down the simplified Boolean equations using K-Map method of reduction. Design a circuit using NOR gates to satisfy this requirement.	**[10]**
2.		Draw a CMOS logic circuit for the given expression. (Assume both true and complementary inputs are available) $F = (A + \overline{CD})(\bar{A} + B).$	**[5]**
3.		Write the Boolean expression for output x in Figure 1. Determine the value of x for all possible input conditions in a truth table.  Figure 1	**[5]**
4.		i. Simplify the given function F1=∑ (1, 5, 6, 7, 11, 12, 13, 15) ii. For the original and the simplified expression, write the Verilog HDL code using dataflow modelling.	**[5] + [5]**
5.		Write a gate level Verilog code for the schematic shown in Figure 2 and write a test bench for the same.	**[10]**

		 Figure 2	
6.		Design a 4:2 priority encoder. Also discuss the differences between encoder and priority encoder?	**[10]**
		Total Marks	**[50]**

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Continuous Assessment Test I – September 2023

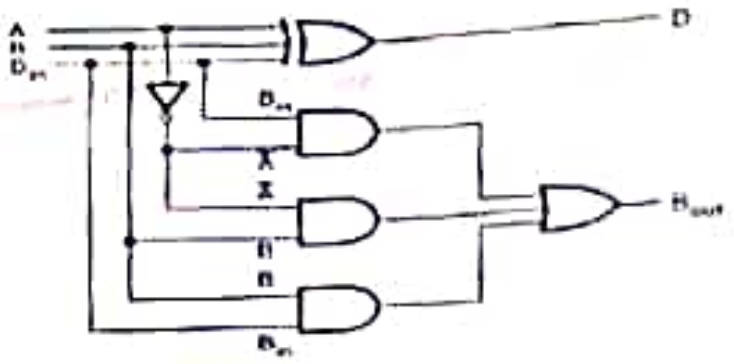
Programme	:	B.Tech.(ECE/ECM)	Semester	:	FALL 2023-24
Course	:	DIGITAL SYSTEM DESIGN	Code	:	BECE102L
			Class Nbr	:	CH2023240100538, CH2023240100368, CH2023240100369, CH2023240100535 CH2023240100365
Faculty	:	Dr Gargi Raina, Dr K Chitra, Dr R Lakshmi, Dr A Prathiba, Dr Jenifer	Slot	:	B1+TB1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1	a)	Simplify the Boolean expression $\overline{A\bar{B}} + \overline{ABC} + A(B + A\bar{B})$	[4]
	b)	Using K-map, simplify the following Boolean function and obtain i) minimal SOP and (ii) minimal POS expressions. $F = \sum_m(0, 2, 3, 6, 7) + \sum_d(8, 10, 11, 15)$	[6]
2	a)	The output of a circuit is 1 if a majority (more than half) of its inputs are equal to 1, and the output is 0 otherwise. Construct a truth table for a three-input majority circuit and design the circuit with NOR gates only	[6]
	b)	Construct the following logic expression using CMOS logic $F = \overline{(A + B + C).D}$	[4]
3	a)	Specify the number of registers and the number of bits per register in the following statement: reg [0:7] name [0:4].	[1]

			[5]

3	b)	Find the output of the test bench shown
		`//dataflow half_adder test bench module`
		`half_adder_df_tb;`
		`reg a, b;`
		`wire sum, cout;`
		`initial`
		`$monitor ("ab = %b, sum = %b, cout = %b", {a, b}, sum, cout);`
		`initial`
		`begin`
		`#10 a = 1'b0;`
		`b = 1'b0;`
		`#10 a = 1'b0;`
		`b = 1'b1;`
		`#10 a = 1'b1;`
		`b = 1'b0;`
		`#10 a = 1'b1;`
		`b = 1'b1;`
		`#10 $stop;`
		`end`
		`half_adder_df inst1 (.a(a), .b(b), .sum(sum), .cout(cout));`
		`endmodule`
				[4]

	c)	Write a Verilog HDL code for the schematic shown  	
4	a)	Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND/OR gates have a propagation delay of 5 ns. What is the total propagation delay time for the full adder circuit? Draw the circuit used for calculation	[3]
	b)	Draw the logic diagram of a 2-to-4-line decoder using universal NAND gates. Include an enable input	[2]
	c)	Implement the following Boolean function with a 4 X 1 multiplexer and external gates $F1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$	[5]
5		Design a 4-input priority encoder and simulate the same using Verilog code with gate primitives. Assume that input D3 has the highest priority	[10]
			Total [50]

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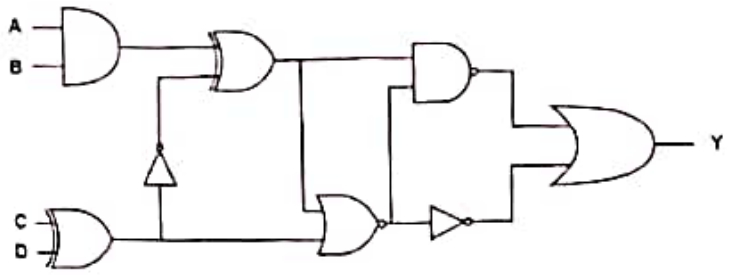
Continuous Assessment Test I – September 2023

Programme	:	B.Tech.(ECE/ECM)	Semester	:	FALL 2023-24
			Code	:	BECE102L
Course	:	DIGITAL SYSTEM DESIGN	Class Nbr	:	CH2023240100388 CH2023240100550 CH2023240100549 CH2023240100406 CH2023240100387 CH2023240100553
Faculty	:	Dr. Kaustab Ghosh,Dr.S.Umadevi,Dr.V.Prakash, Dr.Chandramauleshwar Roy, Dr. Jeans Jenifer, Ms. Hemavathy	Slot	:	B2+TB2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1.		Design a system for switching the lights ON automatically based on the following conditions. 1. If the person is inside the bedroom and the door is closed. 2. If the person is either in the hall or kitchen with the door opened. Reduce the logic using K-map in SOP form and implement the minimized expression using only NAND gates. Consider the door closed to be at logic 1 and the door opened to be at logic 0.	[10]
2.		i) Reduce the following Boolean expression into one literal A'B (D' + C'D) + B (A + A'CD) ii) Construct the following logic expression using static CMOS logic. Y = (A(B+CD))'	[5+5]

3.		For the Verilog HDL code given, assume that the inputs are A=4'b1100, B=4'b1001 C=4'b1010, D=4'b1110, E=2'b10, compute their output F, P, Q, R, S. Show necessary steps involved in computing final output values.
		module test_logic(F,P,Q,R,S,A,B,C,D,E);
		input [3:0]A,B,C,D;
		input [1:0]E;
		output [3:0]F,P,R;
		output [7:0]Q;
		output S;
		reg [3:0]F,P,R;
		reg [7:0]Q;
		reg S;
		always @(A,B,C,D,E)
		begin
			[5]

		F=~(A^B); P=(A<B)?C:D; Q={{2{E}},C}; R=B>>3; S=(C!=D); end endmodule	
4.		The Verilog code to realize the logic diagram of Figure-1 is given below. Analyse this code to identify list of errors in the code and write a new Verilog code by correcting all errors.  **Figure 1** module 2test_gate(Y,A,B,C,D); input A,B,C,D; output Y; Wire W1,W2,W3,W4,W5,W6,W7; and (W1,A,B); xor (W2,C,D); not (W2,W3); xor (W4,W1,W3); nor (W5,W4,W2); nand (W6,W4,W5); nor (Y,W6,W7); endmodule;	[5]
5.		Write a Verilog code for a full-subtractor circuit using dataflow modelling. Assume the circuit has three inputs x, y, B_{in} and two outputs Diff and B_{out}. The circuit subtracts $x - y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and Diff is the difference	[5]
6.		Implement 8:1 Multiplexer using 2:1 Multiplexer	[5]
7.		Assume that you are at the receiving end of a data transmission system, receiving the binary information. You are supposed to receive 3-bit binary numbers with even parity. However, you also need to consider the chances of error due to noise, lesser fan out and other voltage fluctuations in the transmission system. Hence, design a digital circuit which checks whether the received binary information is even parity or not. The circuit needs to be designed based on a truth-table illustrating the parity checking operation and corresponding Karnaugh mapping.	[10]
			Total [50]

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Reg. No.: 22BLC1129

Name : Rishit Pandey

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Continuous Assessment Test I – September 2023

Programme	:	**B.Tech.(ECE/ECM)**	Semester	:	**FALL 2023-24**
			Code	:	**BECE102L**
Course	:	**DIGITAL SYSTEM DESIGN**	Class Nbr	:	**CH2023240100388 CH2023240100550 CH2023240100549 CH2023240100406 CH2023240100387 CH2023240100553**
Faculty	:	**Dr. Kaustab Ghosh,Dr.S.Umadevi,Dr.V.Prakash, Dr.Chandramauleshwar Roy, Dr. Jeans Jenifer, Ms. Hemavathy**	Slot	:	**B2+TB2**
Time	:	**90 Minutes**	Max. Marks	:	**50**

Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1.		Design a system for switching the lights ON automatically based on the following conditions. 1. If the person is inside the bedroom and the door is closed. 2. If the person is either in the hall or kitchen with the door opened. Reduce the logic using K-map in SOP form and implement the minimized expression using only NAND gates. Consider the door closed to be at logic 1 and the door opened to be at logic 0.	[10]
2.		i) Reduce the following Boolean expression into one literal A'B (D' + C'D) + B (A + A'CD) ii) Construct the following logic expression using static CMOS logic. Y = (A(B+CD))'	[5+5]

3.		For the Verilog HDL code given, assume that the inputs are A=4'b1100, B=4'b1001 C=4'b1010, D=4'b1110, E=2'b10, compute their output F, P, Q, R, S. Show necessary steps involved in computing final output values.
		module test_logic(F,P,Q,R,S,A,B,C,D,E);
		input [3:0]A,B,C,D;
		input [1:0]E;
		output [3:0]F,P,R;
		output [7:0]Q;
		output S;
		reg [3:0]F,P,R;
		reg [7:0]Q;
		reg S;
		always @(A,B,C,D,E)
		begin
			[5]

```
F=~(A^B);
P=(A<B)?C:D;
Q={{2{E}},C};
R=B>>3;
S=(C!==D);
end
endmodule
```

4. The Verilog code to realize the logic diagram of Figure-1 is given below. Analyse this code to identify list of errors in the code and write a new Verilog code by correcting all errors. [5]

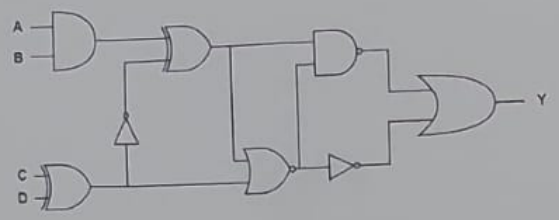


Figure 1

```
module 2test_gate(Y,A,B,C,D);
input A,B,C,D;
output Y;
Wire W1,W2,W3,W4,W5,W6,W7;
and (W1,A,B);
xor (W2,C,D);
not (W2,W3);
xor (W4,W1,W3);
nor (W5,W4,W2);
nand (W6,W4,W5);
nor (Y,W6,W7);
endmodule;
```

5. Write a Verilog code for a full-subtractor circuit using dataflow modelling. Assume the circuit has three inputs x, y, B_{in} and two outputs Diff and B_{out}. The circuit subtracts $x - y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and Diff is the difference [5]

6. Implement 8:1 Multiplexer using 2:1 Multiplexer [5]

7. Assume that you are at the receiving end of a data transmission system, receiving the binary information. You are supposed to receive 3-bit binary numbers with even parity. However, you also need to consider the chances of error due to noise, lesser fan out and other voltage fluctuations in the transmission system. Hence, design a digital circuit which checks whether the received binary information is even parity or not. The circuit needs to be designed based on a truth-table illustrating the parity checking operation and corresponding Karnaugh mapping. [10]

Total [50]

Reg. No.: 22 BLC 1366

Name :

VIT
Vellore Institute of Technology

Continuous Assessment Test I – September 2023

Programme	:	B.Tech.(ECE/ECM)	Semester	:	FALL 2023-24
Course	:	DIGITAL SYSTEM DESIGN	Code	:	BECE102L
			Class Nbr	:	CH2023240100538, CH2023240100368, CH2023240100369, CH2023240100535 CH2023240100365
Faculty	:	Dr Gargi Raina, Dr K Chitra, Dr B Lakshmi, Dr A Prathiba, Dr Jenifer	Slot	:	B1+TB1
Time	:	90 Minutes	Max. Marks	:	50

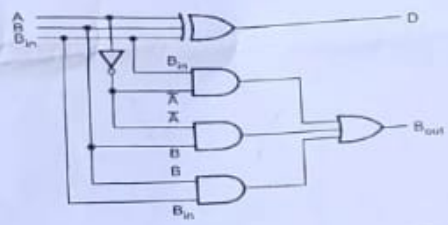
Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1	a)	Simplify the Boolean expression $\overline{A\bar{B} + ABC + A(B + A\bar{B})}$	[4]
	b)	Using K-map, simplify the following Boolean function and obtain i) minimal SOP and (ii) minimal POS expressions. $F = \sum_m(0, 2, 3, 6, 7) + \sum_d(8, 10, 11, 15)$	[6]
2	a)	The output of a circuit is 1 if a majority (more than half) of its inputs are equal to 1, and the output is 0 otherwise. Construct a truth table for a three-input majority circuit and design the circuit with NOR gates only	[6]
	b)	Construct the following logic expression using CMOS logic. $F = \overline{(A + B + C).D}$	[4]
3	a)	Specify the number of registers and the number of bits per register in the following statement: reg [0:7] name [0:4];	[1]

b) Find the output of the test bench shown [5]

```
//dataflow half_adder test bench module
half_adder_df_tb;
reg a, b;
wire sum, cout;
initial
$monitor ("ab = %b, sum = %b, cout = %b", {a, b}, sum, cout);
initial
begin
#10     a = 1'b0;
        b = 1'b0;
#10     a = 1'b0;
        b = 1'b1;
#10     a = 1'b1;
        b = 1'b0;
#10     a = 1'b1;
        b = 1'b1;
#10 $stop;
end
half_adder_df inst1 (.a(a), .b(b), .sum(sum), .cout(cout) );
endmodule
```

c) Write a Verilog HDL code for the schematic shown [4]



4 a) Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND/OR gates have a propagation delay of 5 ns. What is the total propagation delay time for the full adder circuit? Draw the circuit used for calculation [3]

b) Draw the logic diagram of a 2-to-4-line decoder using universal NAND gates. Include an enable input. [2]

c) Implement the following Boolean function with a 4 X 1 multiplexer and external gates. [5]

F1 (A, B, C, D) = $\sum$ (1, 3, 4, 11, 12, 13, 14, 15)

5 Design a 4-input priority encoder and simulate the same using Verilog code with gate primitives. Assume that input D3 has the highest priority [10]

Total [50]

⇔⇔⇔